Digital Electronics

Chapter 1

NUMBER SYSTEMS

Number systems
1.1 Decimal Number system

•*Binary Number system*

•*Octal number system*

•*Hexadecimal Number system*

Decimal Number system
Base/Radix – 10
Ten symbols-0,1,2,3,4,5,6,7,8,9.

1.2 Binary Number system
•*Base/radix – 2(two)*

•*Symbols- 0,1.*

•*One binary digit is called a bit.e.g. o*

•*Nibble: A combination of four bits.e.g.0011*

•*Byte: a combination of eight bits. e.g.10110011*

•*MSB(Most Significant bit)- the leftmost bit of the binary number*

•*LSB(Least Significant Bit)-The rightmost bit of the binary number*

1.3 Octal Number system
•*Base/radix-8*

•*Symbols-0,1,2,3,4,5,6,7.*

1.4 Hexadecimal number system
•*Base/Radix- 16*

•*Symbols : -0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F.*

Chapter 2

Gates

   2. Logic gate

• A **logic gate** is an elementary building block of a digital **circuit**. Most **logic gates** have two or more inputs and one output. At any given moment, every terminal is in one of the two binary conditions low (0) or high (1), represented by different voltage levels.

2.1 Various Logic gates
*AND, OR, NOT, NAND, NOR, EXOR and EXNOR **gates**.*

2.2 Truth Tables
•*Truth tables help understand the behaviour of logic gates.*

•*They show how the input(s) of a logic gate relate to its output(s).*

•*The gate input(s) are shown in the left column(s) of the table with all the different*

possible input combinations. This is normally done by making the inputs count up in binary.

•*The gate output(s) are shown in the right hand side column.*

   2.3 AND Gate*:*
     The output is high if all the inputs are high.It has two or more inputs and one output.

•*Symbol of AND Gate(2 input)*
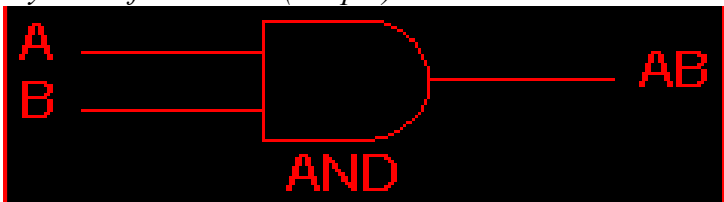
•**Truth table of AND gate**

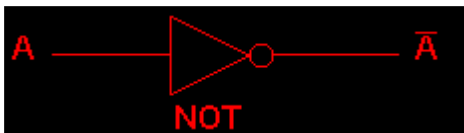| 2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

2.4 OR- GATE:

The output is high if any or all the inputs are high.It has two or more inputs and one output. Symbol of OR gate Truth table of OR gate

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE:
It has one input and one output.
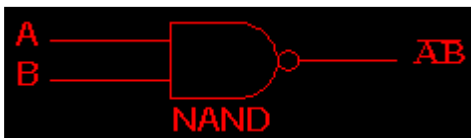

NOT gate	
A	$\overline{A}$
0	1
1	0

The output is complement of the input.

NAND GATE:
The output is high if any of the inputs is low.It has two or more inputs and one output.

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

2.7 NOR GATE
It is NOT-OR gate, If any input is high output is low
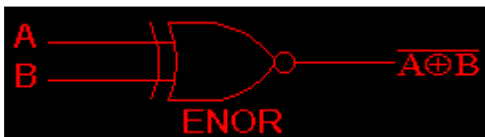*Symbol of 2 input NOR Gate*

Truth Table of NOR Gate

2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

2.8 EX-OR GATE

2 Input EXOR gate		
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

2.9 EX-NOR GATE

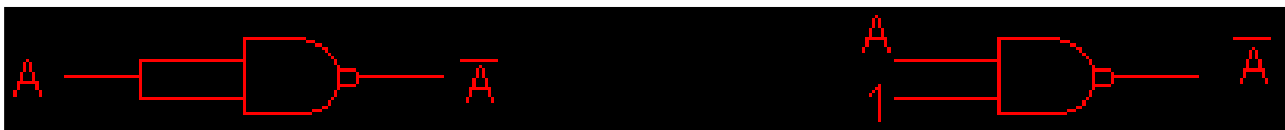| 2 Input EXNOR gate		
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

Symbols of all gates
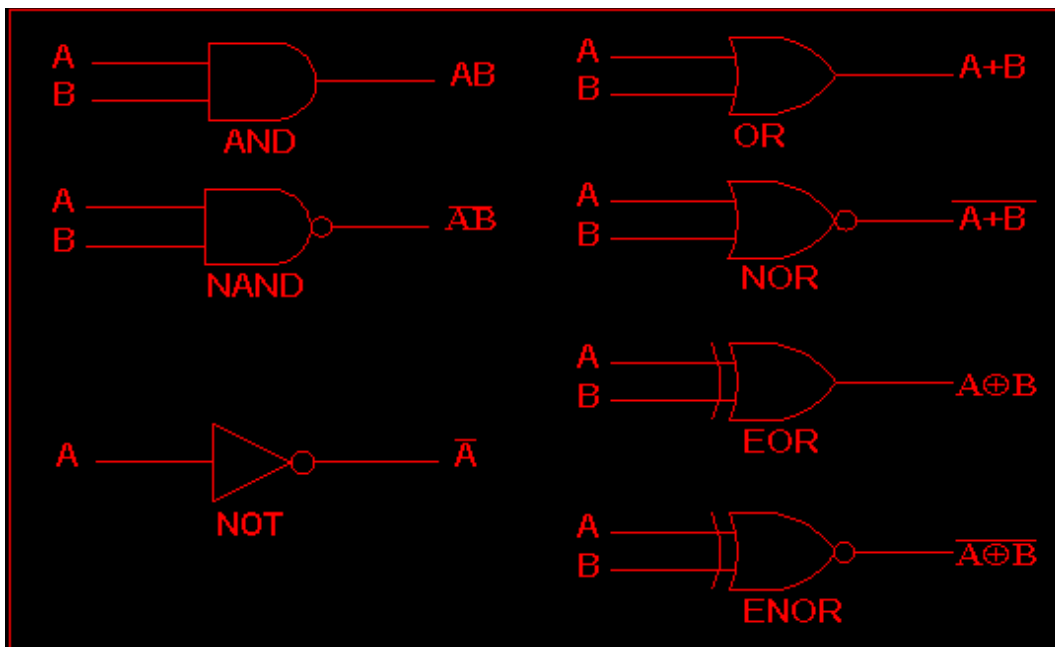
2.10 Universal Gates
NAND Gate
NOR Gate

A NAND gate can be used as a NOT gate using either of the following wiring configurations.

Chapter 3

3.1 Boolean Algebra

ALL the digital circuit operation depend upon only two values that is either 1 or 0 . Where the value of 1 and 0 denoted the predefined voltage level . So , Boolean algebra can used for the analysis , simplification design of digital circuit .

☐ *There are three operation in Boolean Algebra :*

☐ *Logical addition*

☐ *Logical multiplication*

☐ *Logical inversion*

Laws of Boolean Algebra
•Commutative Law

•A+B=B+A(OR Law)

•A.B=B.A(AND Law)

A	B	A+B	B+A
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

Associative Law

•A+(B+C)= (A+B)+C

•A.(B.C)=(A.B).C

A	B	C	A+(B+C)	(A+B)+C
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Distributive Law

•A(B+C)=AB+AC

A	B	C	B+C	A(B+C)	AB	AC	AB+AC
0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	1	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

3.2 DEMORGAN'S THEOREMS

- *A great mathematician named demorgan gives two theorems of Boolean Algebra . These theorems identities used in Boolean Algebra.*

DeMorgan's Theorem #1

A	B	$\overline{A}$ $\overline{B}$	$\overline{A\ B}$		A	B	$\overline{A}+\overline{B}$
0	0	0	1		1	1	1
0	1	0	1		1	0	1
1	0	0	1		0	1	1
1	1	1	0		0	0	0

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

A	B	A + B	$\overline{A + B}$		A	B	$\overline{A}$ x $\overline{B}$
0	0	0	1		1	1	1
0	1	1	0		1	0	0
1	0	1	0		0	1	0
1	1	1	0		0	0	0

3.3 KARNAUGH MAPS (K-MAP)

An n-variable k-map has two cell with each cell corresponding to an n-variable truth table value .

K-Map cell are labeled with the corresponding truth table row .

K-Map cells are arranged such that adjacent cells correspond to truth rows that differ in only one bit position (logical adjacency) .
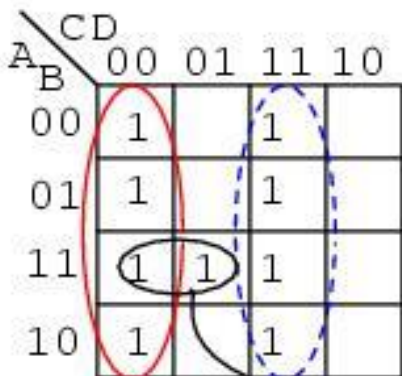
(K-MAPS)

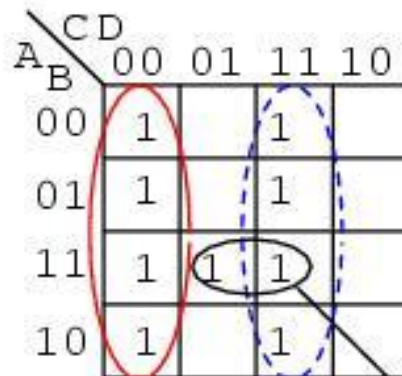*K-Map – A tool for representing Boolean function up to six variables .*

K-Map are tables of row and columns with entries represent 1's or 0's of SOP and POS

representation

Example – 4 variable K-Map

$$Out = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,C\,D + \overline{A}\,B\,\overline{C}\,\overline{D} + \overline{A}\,B\,C\,D + A\,B\,\overline{C}\,\overline{D}$$
$$+ A\,B\,\overline{C}\,D + A\,B\,C\,D + A\,\overline{B}\,\overline{C}\,\overline{D} + A\,\overline{B}\,C\,D$$

$$Out = \overline{C}\,\overline{D} + C\,D + A\,B\,\overline{C}$$

$$Out = \overline{C}\,\overline{D} + C\,D + A\,B\,D$$

Chapter 4

Combinational Circuits

4.1

- **Half Adder (HA).**

- **Full Adder (FA).**

HALF ADDER

Adding two single-bit binary values, X, Y produces a sum S bit and a carry out C-out bit.

This operation is called half addition and the circuit to realize it is called a half adder.
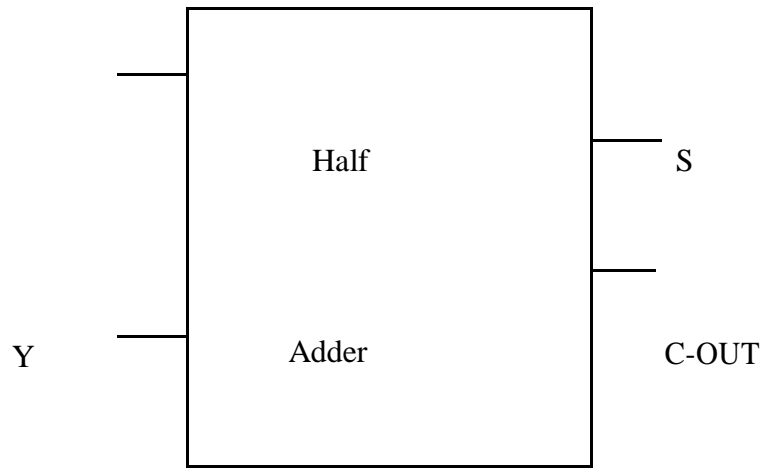
Half Adder Truth Table

Inputs   Outputs

X	Y	S C-out	
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

X

$S(X,Y) = S\ (1,2)$

$S\ \ = X'Y + XY'$
$S = X\ \ Y$

$C\text{-out}(x,\ y,\ C\text{-in}) = S\ (3)$

$C\text{-out} = XY$

FULL ADDER

Adding two single-bit binary values, X, Y with a carry input bit C-in produces a sum bit S and a carry out C-out bit.

Full Adder Truth Table

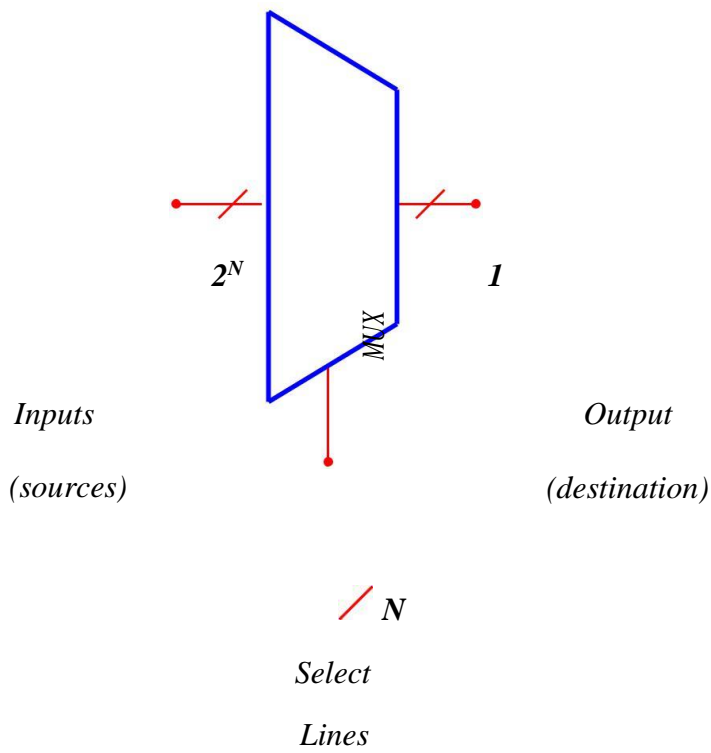| Inputs			Outputs	
X	Y	C-in	S	C-out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

S(X,Y, C-in) = S (1,2,4,7)

C-out(x, y, C-in) = S (3,5,6,7)

4.2 What is a Multiplexer (MUX)?

- *A MUX is a digital switch that has multiple inputs (sources) and a single output (destination).*

- *The select lines determine which input is connected to the output.*

- *MUX Types*

  - *2-to-1 (1 select line)*

  - *4-to-1 (2 select lines)*

  - *8-to-1 (3 select lines)*

  - *16-to-1 (4 select lines)*

    Multiplexer

    Block Diagram

2^N 1

MUX

Inputs   *Output*

(sources)   *(destination)*

N

Select

Lines

What is a Demultiplexer (DEMUX)?

- *A DEMUX is a digital switch with a single input (source) and a multiple outputs (destinations).*

- *The select lines determine which output the input is connected to.*

- *DEMUX Types*

  - *1-to-2 (1 select line)*

  - *1-to-4 (2 select lines)*

  - *1-to-8 (3 select lines)*

  - *1-to-16 (4 select lines)*

Demultiplexer Block Diagram

1   DEMUX   **2^N**

Input   Outputs

(source)   *(destinations)*

N

Select

Lines
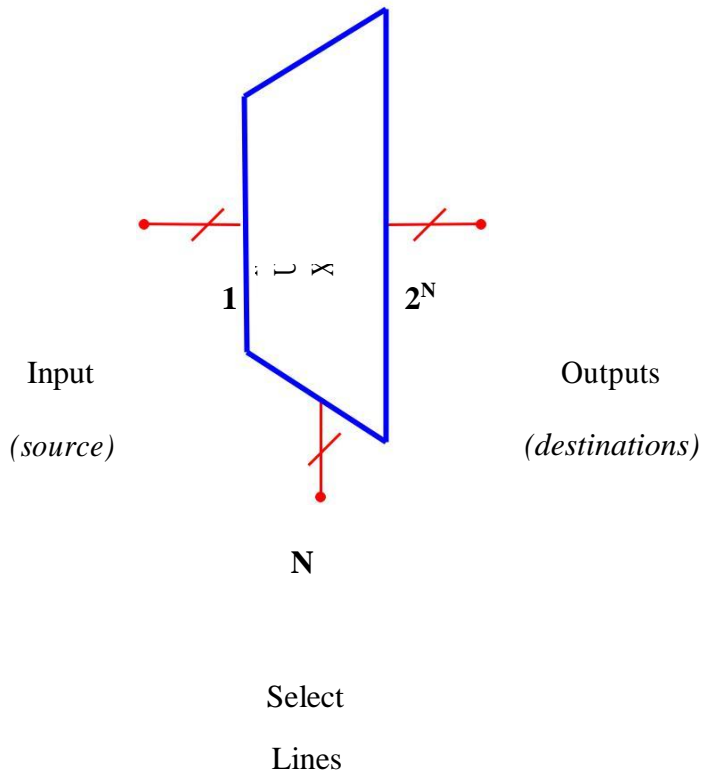
Decoders

A decoder has

$$N \text{ Inputs}$$

$$2^N \text{ Outputs}$$

A decoder selects one of 2^N outputs by decoding the binary value on the N inputs.

The decoder generates all of the minterms of the N input variables.

Encoders

An encoder has

$$2^N \quad inputs \quad N$$
outputs

An encoder outputs the binary value of the selected (or active) input.

An encoder performs the inverse operation of a decoder.

Chapter : 5

FLIP FLOP

☐ *A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs.*

☐ *Flip Flops are sequential circuits.*

☐ *It also stores memory.*

5.1 JK FLIP FLOP

☐ *The **JK flip flop** is basically a gated SR **flip-flop** with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level "1".*

☐ *There is no such thing as a J-K latch, only J-K **flip-flops**.*

☐ *Without the edge-triggering of the clock input, the circuit would continuously **toggle** between its two output states when both J and K were held high (1), making it an astable device instead of a bistable device in that circumstance.*
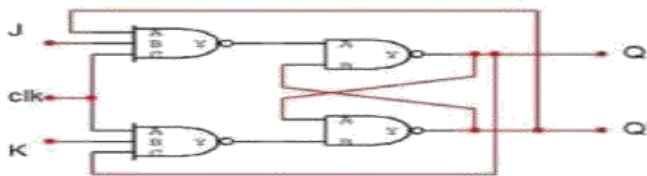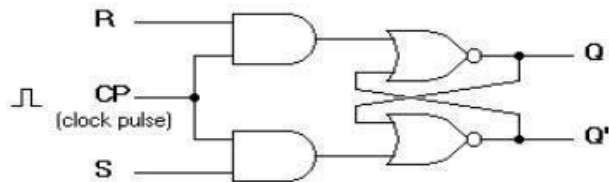

J	K	clk	Q
0	0	1	Önceki konum
0	1	1	0
1	0	1	1
1	1	1	toggle

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

5.2 SR FLIP FLOP

☐ *SR Flip Flop* *is an arrangement of logic gates that maintains a stable output even after the inputs are turned off.*

☐ *This simple flip flop circuit has a set input (S) and a reset input (R).*

(a) Logic diagram

| Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate

(b) Truth table

Clocked SR flip-flop

5.3 D FLIP FLOP

☐ *The **D flip-flop** tracks the input, making transitions with match those of the input **D**.*

☐ *The **D** stands for "data"; this **flip-flop** stores the value that is on the data line.*

☐ *It can be thought of as a basic memory cell. A D **flip-flop** can be made from a set/reset **flip-flop** by tying the set to the reset through an inverter.*

D	Q_{t+1}
0	0
1	1
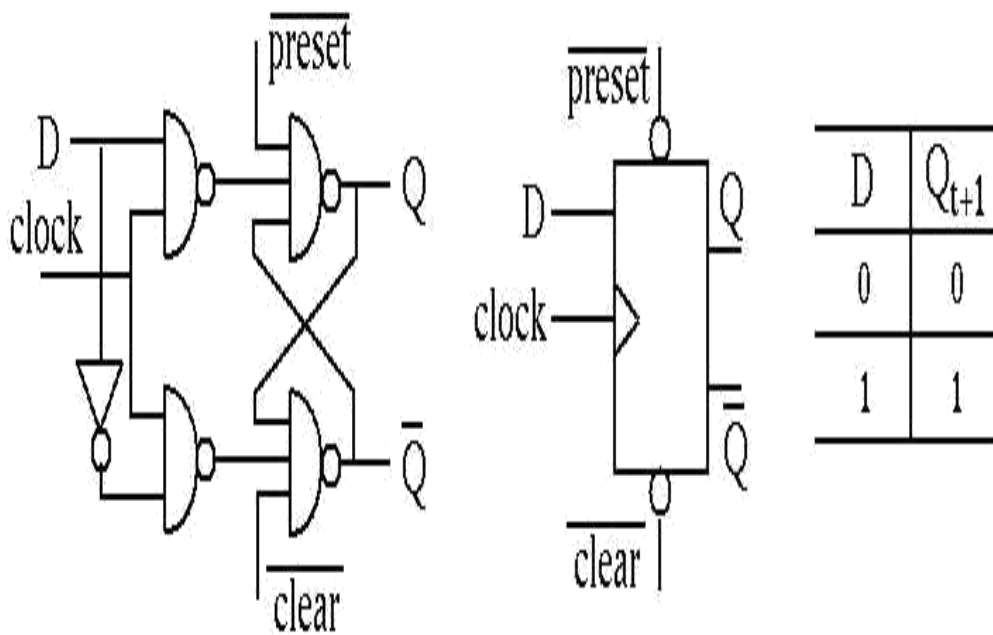
5.4 T or Toggle flip -flop

- *The **T or "toggle" flip-flop** changes its output on each clock edge, giving an output which is half the frequency of the signal **to** the **T** input.*

- *It is useful for constructing binary counters, frequency dividers, and general binary addition devices.*

- *It can be made from a J-K **flip-flop** by tying both of its inputs high.*
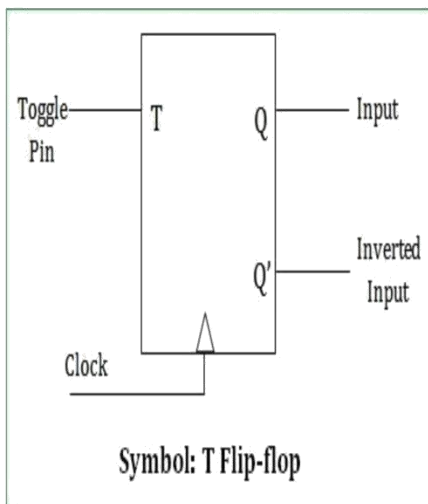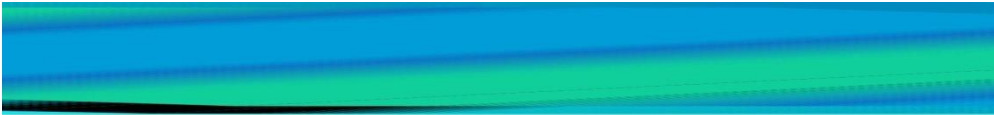
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Symbol: T Flip-flop

5.5 Applications of Flip- Flop

*flip flop** circuit mainly involves in bounce elimination switch.*

data storage, data transfer.

latch, registers, counters.

frequency division, memory, etc

Chapter 6
Introduction of Shift Register & Counters

Counter is the combination of flip-flop which is used to count the events of number of clock at input. Depending upon the manner by mean of which the flip-flop of counter triggered.

　　　　□　　*There is two types of counters:*

　　　　　　□　　*Asynchronous Counter*

　　　　　　□　　*Synchronous Counter*

ASYNCHRONOUS COUNTER

□　*Asynchronous counters are **those whose output is free from the clock signal**. Because the flip flops in asynchronous counters are supplied with different clock signals, there may be delay in producing output. The required number of logic gates to design asynchronous counters is very less. So they are simple in design.*

SYNCHRONOUS COUNTER

□　*In synchronous counters, the **clock inputs of all the flip-flops** are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel).*

Counters

* Applications include:
  - system clock
  - timer, delays
  - watches, clocks, alarms
  - counting events
  - memory addressing
  - frequency division
  - sequence control
  - cycle control
  - protocols

Present State		Next State	
A	B	A	B
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0
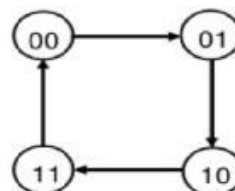
Shift Register

- A <u>register</u> is a digital circuit with two basic functions: Data Storage and Data Movement
  - A <u>shift register</u> provides the data movement function
  - A shift register "shifts" its output once every clock cycle

- A shift register is a group of flip-flops set up in a linear fashion with their inputs and outputs connected together in such a way that the data is shifted from one device to another when the circuit is active

Types of Shift Register

☐ *SERIAL IN SERIAL OUT (SISO)*

☐ *SERIAL IN PARALLEL OUT (SIPO)*

☐ *PARALLEL IN SERIAL OUT (PISO)*

☐ *PARALLEL IN PARALLEL OUT (PIPO)*

Shift Register Applications

- converting between serial data and parallel data
- temporary storage in a processor
  - scratch-pad memories
- some arithmetic operations
  - multiply, divide
- communications
  - UART
- some counter applications
  - ring counter
  - Johnson counter
  - Linear Feedback Shift Register (LFSR) counters
- time delay devices
- more ...

3
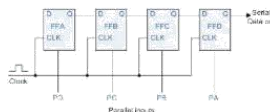
Chapter 7

A/D and D/A Convertors

7.1 What is A/D Convertor

☐ *An electronic integrated circuit which transforms a signal from analog (continuous) to digital (discrete) form.*

☐ *Analog signals are directly measurable quantities.*

☐ *Digital signals only have two states. For digital computer, we refer to binary states, 0 and 1.*

Successive Approximation

☐ *Uses a n-bit DAC to compare DAC and original analog results.*

☐ *Uses Successive Approximation Register (SAR) supplies an approximate digital code to DAC of Vin.*

☐ *Comparison changes digital output to bring it closer to the input value.*

D/A Convertors

A digital to analog converter (DAC) converts a digital signal to an analog voltage or current output.

Types of DACs

☐ *Many types of DACs available.*

☐ *Usually switches, resistors, and op-amps used to implement conversion*

☐ *Two Types:*

  ☐ *Binary Weighted Resistor*

  ☐ *R-2R Ladder*

Binary Weighted Resistor

- *Utilizes a summing op-amp circuit*

- *Weighted resistors are used to distinguish each bit from the most significant to the least significant*

- *Transistors are used to switch between V_{ref} and ground (bit high or low)*

Chapter 8

Semi- Conductor Memories

Memory Organization

- *It provides spaces for storing instruction and data, space for intermediate results and spaces for final results.*

- *Memory is primarily of two types;*

- *(a) INTERNAL MEMORY: Primary/Main Memory And Cache Memory.*
- *(b) EXTERNAL MEMORY: Secondary Storage.*

INTERNAL MEMORY

- PRIMARY

Primary memory is computer memory that a processor or computer accesses first or directly. It allows a processor to access running execution applications and services that are temporarily stored in a specific memory location. Primary memory is also known as primary storage or main memory

- CACHE MEMORY

Cache memory is a small-sized type of volatile computer memory that provides high-speed data access to a processor and stores frequently used computer programs, applications and data. It is the fastest memory in a computer

External Memory

The storage capacity of the main memory or the primary memory of the computer is limited. Sometimes we have to store millions or billions bytes of data and primary memory of this computer is not able to store this data. Therefore, we require additional memory called auxiliary memory or secondary storage.

SEMICONDUCTOR MEMORY

semiconductor memories are small in size, have low cost, high speed of operation, high reliability and memory size can be expanded according to their requirements.

WHAT IS ROM?

*Read-only memory (**ROM**) is a type of storage medium that permanently stores data on personal computers (PCs) and other electronic devices. It contains the programming needed to start a PC, which is essential for boot-up; it performs major input/output tasks and holds programs or software instructions.*

TYPES OF ROM:-

1.   *Programmable Read Only Memory[PROM]*

2.   *Erasable Programmable Read Only Memory [EROM]*

3.   *Electrical Erasable Programmable Memory [EEPROM]*

WHAT IS RAM?

*Random Access Memory (**RAM**) is the hardware in a computing device where the operating system (OS), application programs and data in current use are kept so they can be quickly reached by the device's processor. **RAM** is the main memory in a computer, and this type of memory is volatile and all information that was stored in **RAM** is lost when computer is turned off.*

TYPES OF RAM

1.STATIC RAM

*SRAM (**Static RAM**) is random access memory (**RAM**) that retains data bits in its memory as long as power is being supplied.*

2.DYNAMIC RAM

Dynamic RAM (DRAM), which stores bits in cells consisting of a capacitor and a transistor

Very Short Answer type questions.

(a) Indirect rangıng.

(b) $(1101101)_2 = ($ $)_2$

(c) 2's complement of 1101101 is_____

(d) Old Parity

(e) Truth table of 2 input NAND gate

(f) Expand CMOS

(g) Expand EPROM

(h) What is A to D Converter

(i) Applications of MUX

(j) Draw D flip flop

(k) Synchronous counter

(l) PIP0

(m) Encoder

(n) Truth table of half adder

(o) Draw symbol of Ex-OR gate

(p) Prove $A + ABA+B$

(q) How many variables get eliminated by making a group of four.

(r) IC of ALU is

Short Answer type questions.

1. Write advantages of Digital signals.

2. Explain concept of Parity in error detection and correction.

3. Explain the working of TTL NAND gate

4.State and explain De-Morgan's theorem

5. Explain working of half adder with it's truth table.

6. Explain the working of R-S flip-flop

7. Explain the concept of race around condition in flip-flo

8. What is the difference between a latch and a flip-flop

9. Write a note on Asynchronous counter

10. Explain the working of sIPO shift register.

11. Explain working of Dual slope A to D converter

12. What is the difference between static and dynamic RAM

13. Explain working of R/2R ladder D to A converter

14 Explain working of IC74181 ALU

15. Explain the working of 7 segment display decoder circuit.

Long Answer type questions.

Q.1. Explain the working of universal shift register.

Q.2. Explain the working of successive approximation A to D converte

Q.3. Solve the Boolean expression

$f(A, B, C, D)=\sum(10, 1, 3, 5,6,7, 10, 14, 15)$

by using k-map

Q.4. Write a short note on any two

(i) CMOS logic family

(ii) Encoder

(iii) Application of A/D converter.